Chapter 3
–Transceiver BS8 –
BS8_RF Block

AMENDMENT RECORD SHEET

Amendment Number	Date	Inserted By	Comments
	02/99		Original

CONTENTS – RF

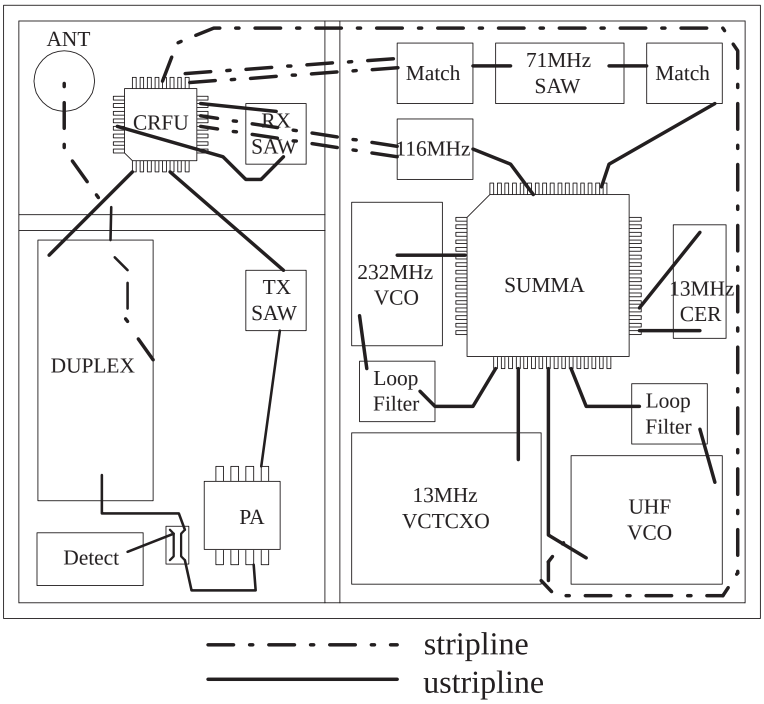
Introduction

This document defines the RF–module of the RAE–2 GSM–"engine". This section contains electrical specifications, functional descriptions, block diagrams etc.

Technical summary

The RF in the RAE–2 GSM is based on the architecture used in DCT 3.

The RAE–2 RF Engine (figure below) is a single side design, on the A–side, with all components located under the PDA unit. Shielding comprises three shielding cans with removable lids. The maximum building height for the RF Engine is 2 mm.



RF Characteristics

Table 1. Main RF characteristics

Item	Values
Receive frequency range	935 ... 960 MHz
Transmit frequency range	890 ... 915 MHz
Duplex spacing	45 MHz
Channel spacing	200 kHz

Table 1. Main RF characteristics (continued)

Item	Values
Number of RF channels	124
Power class	4
Number of power levels	15

Note 1 : Standard of primary GSM 900 Band, **P – GSM**

890 – 915 MHz : Mobile transmit, Downlink
935 – 960 MHz : Mobile receive, Uplink

Transmitter Characteristics

Item	Values
Type	Upconversion, nonlinear, FDMA/TDMA
Intermediate frequency (phase modulated)	116 MHz
LO frequency range	1006 ... 1031 MHz
Output power	2 W peak (33 dBm)
Power control range	min. 5 ... 33 dBm
Maximum phase error (RMS/peak)	max 5 deg./20 deg. peak

Output power

Parameter	Min.	Typ.	Max.	Unit / Notes
Max. output power		33.0		dBm
Max. output power tolerance (power level 5)			+/– 2.0 +/– 2.5	dB, normal cond. dB, extreme cond.
Output power tolerance / power levels 6...15			+/– 3.0 +/– 4.0	dB, normal cond. dB, extreme cond.
Output power tolerance / power levels 16...19			+/– 5.0 +/– 6.0	dB, normal cond. dB, extreme cond.
Output power control step size	0.5	2.0	3.5	dB

Note 1 : Output power refers to the measure of power when averaged over the useful part of the burst. Power levels are measured at the antenna connector.

Note 2 : Interval between power steps shall be 2 +/–1.5 dB

Receiver characteristics

Item	Values
Type	Linear, FDMA/TDMA
IF frequencies	1st 71 MHz, 2nd 13 MHz
LO frequencies	1st LO 1006 ... 1031 MHz, 2nd LO 58 MHz
Typical 1 dB bandwidth	+/– 90 kHz
Sensitivity	min. – 102 dBm , S/N >8 dB
Total typical receiver voltage gain (from antenna to RX ADC)	73 dB
Receiver output level (RF level –95 dBm)	50 mVpp (typical balanced signal level of 13 MHz IF in RF BB interface = input level to RX ADCs)
Typical AGC range (dynamic range –93dB)	–17 ... +40 dB
Accurate AGC control range	57 dB
Typical AGC step in LNA	–15 dB
Usable input dynamic range	–102 ... –10 dBm
RSSI dynamic range	–110 ... –48 dBm
AGC relative accuracy on channel (accurate range)	+/– 0.8 dB
Compensated gain variation in receiving band	+/– 1.0 dB

DC characteristics

Regulators

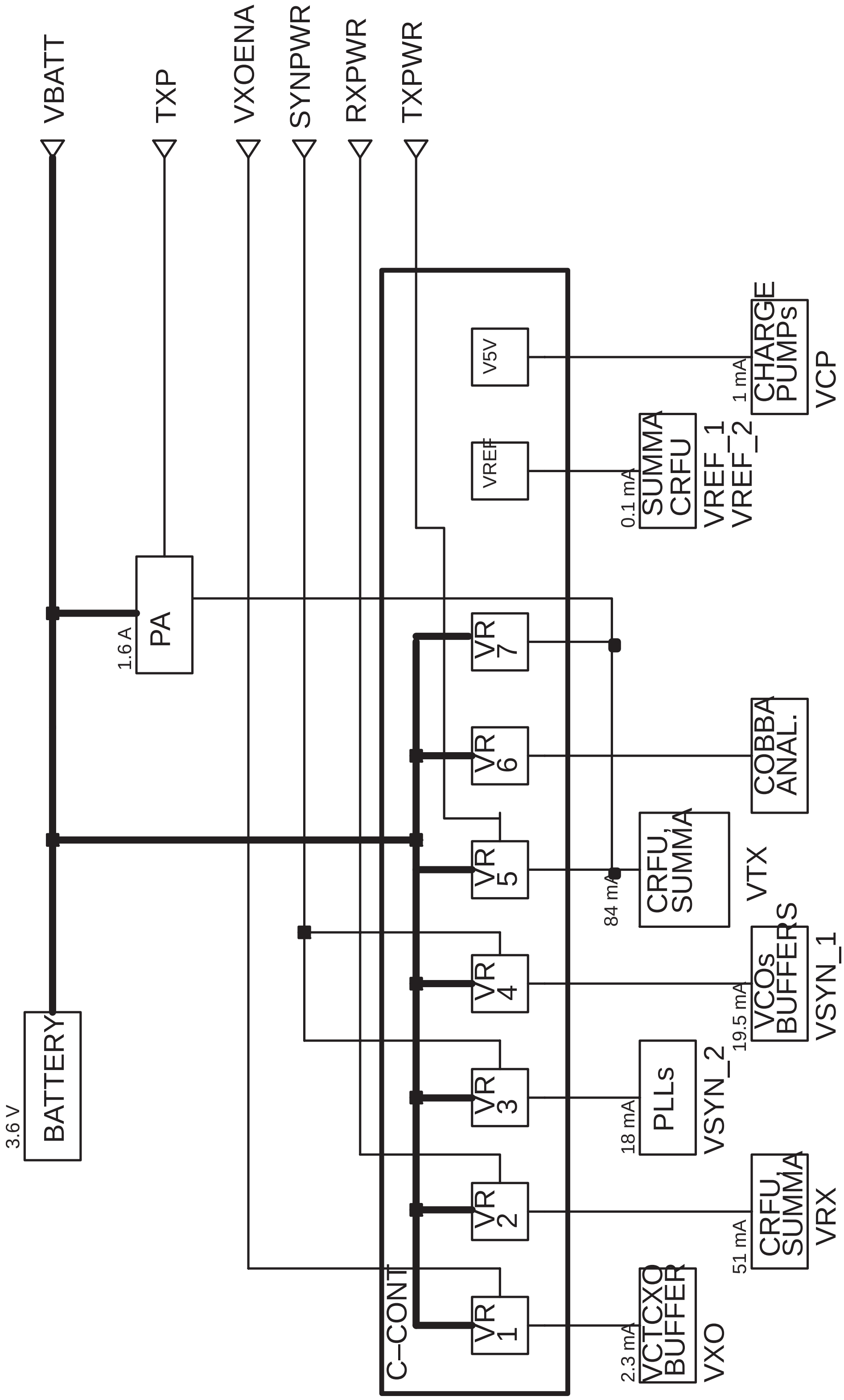
Transceiver has got a multi function power management IC, which contains among other functions, also 7 pcs of 2.8 V regulators. All regulators can be controlled individually with 2.8 V logic directly or through control register. In GSM direct controls are used to get fast switching, because regulators are used to enable RF–functions.

Use of the regulators can be seen in the power distribution diagram.

CCONT also provides 1.5 V reference voltage for SUMMA and CRFU1a (and for DACs and ADCs in COBBA too).

All control signals are coming from MAD and they are 2.8 V logic signals..

Power distribution diagram



Functional descriptions

RF block diagram

The RF block comprises a conventional dual conversion receiver and the transmitter features an up–conversion mixer for the final TX–frequency.

The architecture contains three ICs. Most of the functions are horizontally and vertically integrated. UHF functions except power amplifier and VCO are integrated into CRFU_1a, which is a BiCMOS–circuit suitable for LNA– and mixer–function. Most of the functions are in SUMMA, which also is a BiCMOS–circuit. SUMMA is a IF–circuit including IQ–modulator and PLLs for VHF– and UHF–synthesizers.

Power amplifier is also an ASIC, it is a so called MMIC (monolithic microwave integrated circuit). It has got three amplifier stages including input and interstage matchings. Output matching network is external. Also TX gain control is integrated into this chip.

See block diagram next page

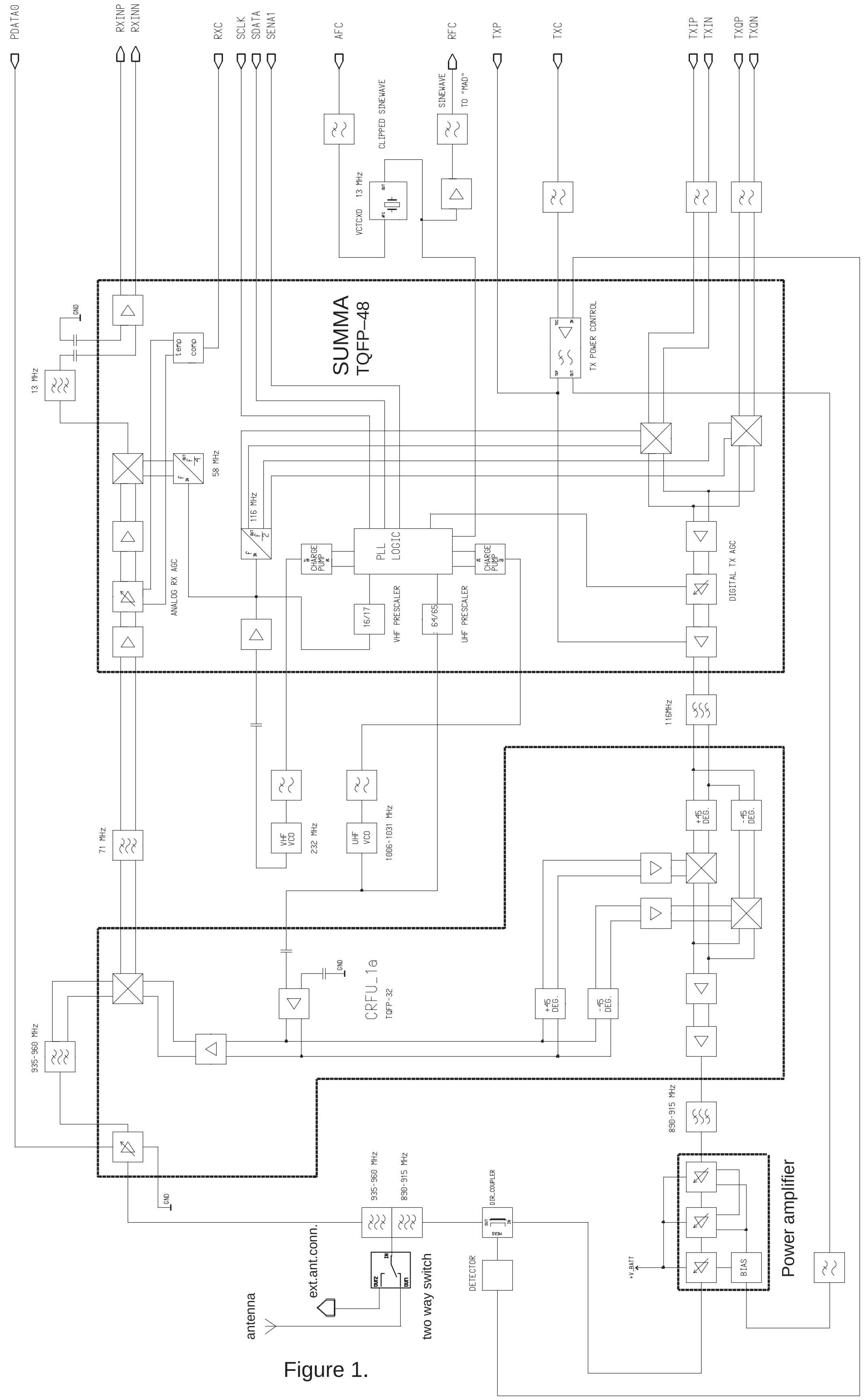

PDATA0
RXINP
RXINN
RXC
SCLK
SDATA
SENA1
AFC
RFC
TXP
TXC
TXIP
TXIN
TXQP
TXQN
CLIPPED SINEWAVE
SINEWAVE
TO "MAD"
VCTCXO 13 MHz
SUMMA
TQFP–48
TX POWER CONTROL
13 MHz
58 MHz
116 MHz
PLL
LOGIC
CHARGE PUMP
16/17
64/65
VHF PRESCALER
UHF PRESCALER
ANALOG RX AGC
DIGITAL TX AGC
116MHz
71 MHz
VHF VCO
232 MHz
UHF VCO
1006-1031 MHz
+45 DEG.
-45 DEG.
CRFU_1a
TQFP-32
935-960 MHz
890-915 MHz
DIR_COUPLER
DETECTOR
BIAS
Power amplifier
antenna
ext.ant.conn.
two way switch

Figure 1.

Frequency synthesizers

Both VCOs are locked with PLLs into stable frequency source, which is a VCTCXO–module (voltage controlled temperature compensated crystal oscillator). The VCTCXO is running at 13 MHz. Temperature effect is controlled with AFC (automatic frequency control) voltage, the VCTCXO is locked into the frequency of the base station. AFC is generated by baseband with a 11 bit conventional DAC in COBBA.

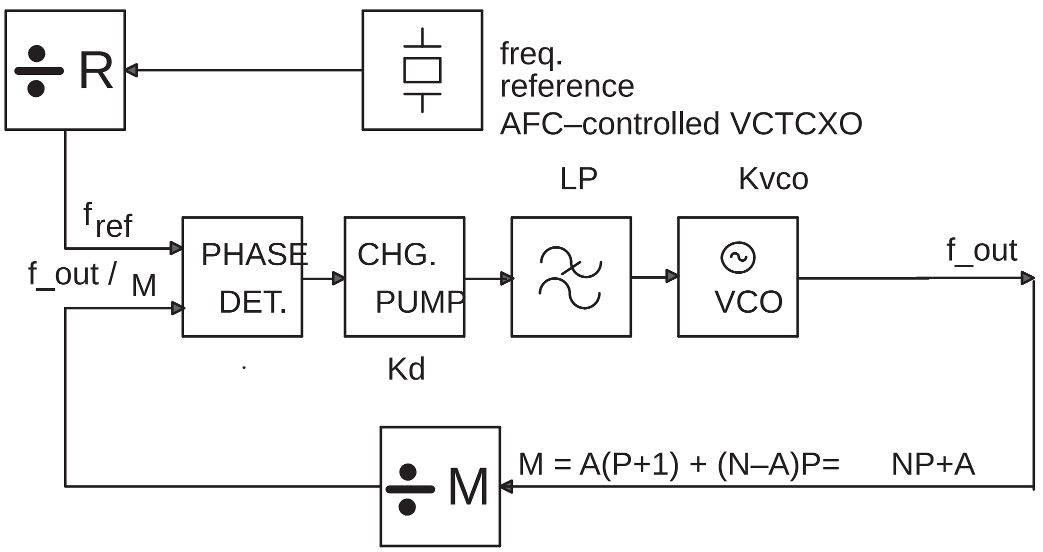
The UHF PLL is located in the SUMMA. There is 64/65 (P/P+1) prescaler, N– and A–divider, reference divider, phase detector and charge pump for the external loop filter.

The UHF local signal is generated by a VCO–module (VCO = voltage controlled oscillator) and sample of frequency of VCO is fed to prescaler. The prescaler is a dual modulus divider. The output of the prescaler is fed to the N– and A–dividers, which produce the input to phase detector.

The phase detector compares this signal to reference signal, which is divided with reference divider from VCTCXO output. Output of the phase detector is connected into charge pump, which charges or discharges integrator capacitor in the loop filter depending on the phase of the measured frequency compared to reference frequency.

The loop filter filters out the pulses and generates the DC to control the frequency of UHF–VCO. The loop filter defines step response of the PLL (settling time) and effects to stability of the loop, that’s why integrator capacitor has got a resistor for phase compensation.

The other filter components are for sideband rejection. Dividers are controlled via serial bus. SDATA is for data, SCLK is serial clock for the bus and SENA1 is a latch enable, which stores new data into dividers. The UHF–synthesizer is the channel synthesizer, so the channel spacing is 200 kHz. 200 kHz is the reference frequency for the phase detector.



VHF PLL is also located into SUMMA. It comprises a 16/17 (P/P+1) dual modulus prescaler, N– and A–dividers, reference divider, phase detector and charge pump for the loop filter. The VHF local signal is generated with a discrete VCO–circuit. The VHF PLL works in the same way as UHF–PLL. The VHF–PLL is locked on fixed frequency, so higher reference frequency is used to decrease phase noise.

Receiver

Receiver is a dual conversion linear receiver.

The received RF–signal from the antenna is fed via the duplex filter to LNA (low noise amplifier) in CRFU_1a. Active parts (RF–transistor and biasing and AGC–step circuitry) are integrated into this chip. Input and output matching networks are external.

Gain selection is carried out with PDATA0 control. Gain step in LNA is activated when the RF–level in the antenna is about –45 dBm.

After the LNA amplified signal (with low noise level) is fed to bandpass filter, which is a SAW–filter (SAW, surface acoustic wave).

This bandpass filtered signal is then mixed down to 71 MHz, which is the first intermediate frequency. The 1st mixer is located into CRFU_1a ASIC. This integrated mixer is a double balanced Gilbert cell. All active parts and biasing are integrated and matching components are external. Because this is an axtive mixer it also amplifies IF–frequency. Also local signal buffering is integrated and upper side injection is used. First local signal is generated by the UHF–synthesizer.

The first IF–signal is then bandpass filtered with a selective SAW–filter. From the mixer output to the IF–circuit input the signal path is balanced. The IF–filter provides selectivity for channels greater than +/–200 kHz. Also it attenuates image frequency of the second mixer and intermodulating signals. Selectivity is required in this place, because of needed linearity and adjacent channel interferers will be on too high signal level for the stages following.

The next stage in the receiver chain is AGC–amplifier. It is integrated into SUMMA–ASIC. The AGC has got analog gain control. The control voltage for the AGC is generated with DA–converter in COBBA in baseband. AGC–stage provides accurate gain control range (min. 57 dB) for the receiver.

After the AGC there is the second mixer, which generates the second intermediate frequency, 13 MHz. The local signal is generated in SUMMA by dividing VHF–synthesizer output (232 MHz) by four, so the 2nd LO–frequency is 58 MHz.

The 2nd IF–filter is a ceramic bandpass filter at 13 MHz. It attenuates adjacent channels, except for +/– 200 kHz there is not much attenuation. Those +/– 200 kHz interferers are filtered digitally by the baseband. So the RX DACs are so good, that there is enough dynamic range for the faded 200 kHz interferer. Also the whole RX has to be able to handle signal levels in a linear way

After the 13 MHz filter there is a buffer for the IF–signal, which also converts and amplifies single ended signal from filter to balanced signal for the buffer and AD–converters in COBBA. Buffer in SUMMA has got voltage gain of 36dB and buffer gain setting in COBBA is 0 dB. It is possible to set gainstep (9.5 dB) into COBBA via control bus, if needed..

Transmitter

The transmitter chain consists of IQ–modulator, upconversion mixer, power amplifier and there is a power control loop.

I– and Q–signals are generated by baseband in COBBA–ASIC. After post filtering (RC–network) they are fed into IQ–modulator in SUMMA. It generates modulated TX IF–frequency, which is VHF–synthesizer output divided by two, that is 116 MHz. The TX–amplifier in SUMMA has two selectable gain levels. Output is set to maximum via control register of SUMMA. After SUMMA there is a bandpass LC–filter for noise and harmonic filtering before the signal is fed for upconversion into final TX–frequency in CRFU_1a.

Upconversion mixer in CRFU_1a is a so called image reject mixer. It attenuates the unwanted sideband in the upconverter output. The mixer itself is a double balanced Gilbert cell. The phase shifters required for image rejection are also integrated. The local signal needed in upconversion is generated by the UHF–synthesizer, but buffers for the mixer are integrated into CRFU_1a.

The output of the upconverter is buffered and matching network makes a single ended 50 ohm impedance.

The next stage is a TX interstage filter, which attenuates the unwanted signals from the upconverter, mainly LO–leakage and image frequency from the upconverter. Also it attenuates the wideband noise. This bandpass filter is a SAW–filter.

The final amplification is carried out by the third IC, the power amplifier which is a MMIC. It features a 50 ohm input, output requires an external matching network. The MMIC comprises three amplifier stages and interstage matchings. Also included is a gain control, which is controlled with a power control loop. The PA features over 35 dB power gain and it is able to produce 2.5 W into output with 0 dBm input level. The gain control range is over 35 dB to get desired power levels and power ramping up and down.

The harmonics generated by the nonlinear PA (class AB) are filtered out with the matching network and lowpass/bandstop filtering in the duplexer. Bandstop is required because of wideband noise located on RX–band.

Power control circuitry consists of a power detector in the PA output and an error amplifier in SUMMA. There is a directional coupler connected between the PA–output and the duplex filter. It takes a sample from the forward going power with certain ratio. This signal is rectified in a schottky–diode and it produces a DC–signal signal after filtering. This peak–detector is linear on absolute scale, except it saturates on very low and high power levels – it produces a S–shape curve.

This detected voltage is compared in the error–amplifier in SUMMA to TXC–voltage, which is generated by DA–converter in COBBA. Because also gain control characteristics in PA are linear in absolute scale, control loop defines a voltage loop, when closed. The closed loop tracks the TXC–voltage quite linearly.

The TXC has got a raised cosine form ($\cos^4$ – function), which reduces switching transients, when pulsing power up and down. Because dynamic range of the detector is not wide enough to control the power (actually RF output voltage) over the whole range, there is a control named TXP to work under detected levels. Burst is enabled and set to rise with the TXP until the output level is high enough, that feedback loop works. The loop controls the output via the control pin in the PA MMIC to the desired output level and burst has got the waveform of TXC–ramps. Because feedback loops could be unstable, this loop is compensated with a dominating pole. This pole decreases gain on higher frequencies to get phase margins high enough.

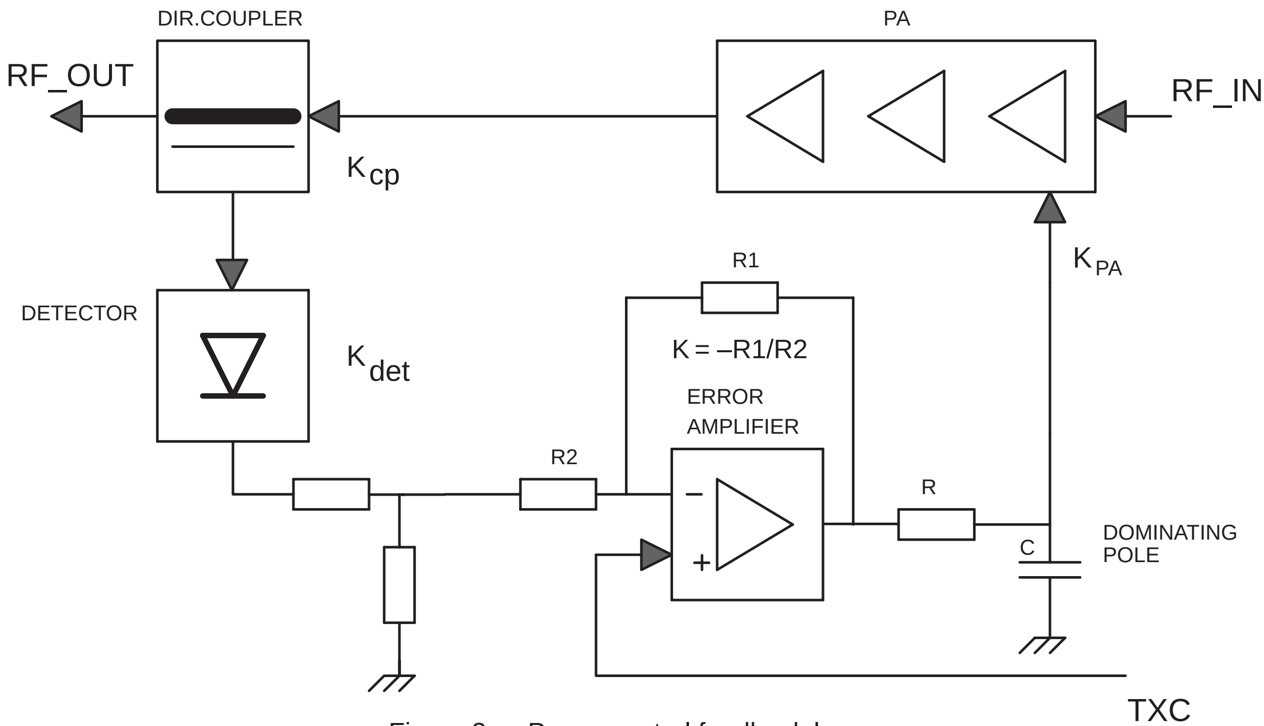


Figure 2. Power control feedback loop

AGC strategy

The AGC–amplifier is used to maintain output level of the receiver almost constant.

AGC has to be set before each received burst, this is called pre–monitoring. The receiver is switched on before the burst begins, the DSP measures received signal level and adjusts RXC, which controls RX AGC–amplifier or it switches off the LNA with PDATA0 control line. This pre–monitoring is done in three phases and this sets the settling times for RX AGC. Pre–monitoring is required because of linear receiver, received signal must be in full swing, no clipping is allowed and because DSP doesn't know, what is the level going to be in next burst.

There is at least 60 dB accurate gain control (continuous, analog) and one digital step in LNA. It is typically about 30...35 dB.

RSSI must be measured on range –48...–110 dBm. After –48 dBm level MS reports to base station the same reading.

Because of RSSI–requirements, gain step in LNA is used roughly on –45 dBm RF–level and up to –10 dBm input RF–level accurate AGC is used to set RX output level. LNA is ON (PDATA0 = ”0”) below –47 dBm. from –47 dBm down to –95 dBm

This accurate AGC in SUMMA is used to adjust the gain to desired value. RSSI–function is in DSP, but it works out received signal level by measuring RX IQ–level after all selectivity filtering (meaning IF–filters, $\Sigma\Delta\pm$converter and FIR–filter in DSP). So 50 dB accurate AGC dynamic range is required. Remaining 10 dB is for gain variations in RX–chain (for calibration)

Below –95 dBm RF–levels, output level of the receiver drops dB by dB. At –95 dBm level output of the receiver gives 50 mVpp. This is the target value for DSP. Below this it drops down to ca. 9 mVpp @ –110 dBm RF–level.

This strategy is chosen because we have to roll off the AGC in PLUSSA early enough, that it won't saturate in selectivity tests. Also we can't start too early, then we will sacrifice the signal to noise ratio and it would require more accurate AGC dynamic range. 50 mVpp target level is set, because RX–DAC will saturate at 1.4 Vpp. This over 28 dB headroom is required to have margin for +/– 200 kHz faded adjacent channel (ca. 19 dB) and extra 9 dB for pre–monitoring.

Production calibration is done with two RF–levels, LNA gain step is not calibrated. The gain changes in the receiver are taken off from the dynamic range of accurate AGC. Variable gain stage in SUMMA is designed in a way, that it is capable of compensating itself, there is good enough margin in AGC.

AFC function

AFC is used to lock the transceivers clock to the frequency of the base station.

AFC–voltage is generated in the COBBA with a 11 bit AD–converter. There is a RC–filter in AFC control line to reduce the noise from the converter. Settling time requirement for the RC–network comes from signalling, how often PSW (pure sine wave) slots occur. They are repeated after 10 frames , meaning that there is PSW in every 46 ms.

AFC tracks the base station frequency continuously, so the transceiver has got a stable frequency, because changes in the VCTCXO–output don't occur so fast (temperature).

Settling time requirement comes also from the start up–time allowed. When transceiver is in sleep mode and ”wakes” up to receive mode , there is only about 5 ms for the AFC–voltage to settle. When the first burst comes in system clock has to be settled into +/– 0.1 ppm frequency accuracy. Settling time requirement comes also from the start up–time allowed. When transceiver is in sleep mode and ”wakes” up to receive mode , there is only about 5 ms for the AFC–voltage to settle. When the first burst comes in system clock has to be settled into +/– 0.1 ppm frequency accuracy.

The VCTCXO–module requires also 5 ms to settle into final frequency. Amplitude rises into full swing in 1 ... 3 ms, but frequency settling time is longer so this oscillator must be powered up early enough.

RF block requirements

Duplex filter

Parameter	Transmit section		Receive section		unit
Center frequency, ftx,frx	ftx : 902.5		frx : 947.5		MHz
BW (bandwidth) at passband	+/– 12.5		+/– 12.5		MHz
Maximum insertion loss at BW	1.6 (at +25 deg. C) 1.9 (at –20...+85 deg. C)		3.2 (at +25 deg. C) 3.7 (at –20...+85deg. C)		dB
Ripple at BW, peak to peak	1.1		1.5		dB
Terminating impedance	50		50		ohms
Maximum VSWR	2.2		1.8		
Minimum attenuations	Freq.range	Att.	Freq.range	Att.	
	925...935	3	3...200	30	MHz/dB
	935...960	15	200...500	16	MHz/dB
	1780...1830	28	500...890	25	MHz/dB
	2670...2745	35	890...915	26	MHz/dB
			980...1000	21	MHz/dB
			1000...1050	23	MHz/dB
			1400...1500	35	MHz/dB
Permissible input power	4.0 AVG (12.5% duty cyclr)				W

Part no: NMP code 4512075

Receiver blocks

LNA in CRFU_1a

Parameter	Min.	Typ.	Max.	Unit/Notes
Frequency band	935 – 960			MHz
Supply voltage	2.7	2.8	2.855	V
Current consumption			8	mA
Insertion gain	17.5	18.5	19.5	dB
Noise figure		1.7	2.2	dB,PDATA0=H
Input 1 dB compression point	–19			dBm, PDATA0=H
Reverse isolation	15			dB
Input VSWR			2	

Parameter	Min.	Typ.	Max.	Unit/Notes
Output VSWR			2	
Gain reduction	30		35	dB,room temp.
Step accuracy	–2		+2	dB,over temp.range
Noise figure, when PDATA=0		20		dB

RX interstage filter

Parameter	Min.	Typ.	Max.	Unit
Passband	935 – 960			MHz
Insertion loss			3.3	dB
Ripple in passband			1.3	dB
Attenuation DC...890 MHz	45			dB
Attenuation 890...915 MHz	25			dB
Attenuation 980...1030 MHz	25			dB
Attenuation 1025...3000 MHz	35			dB
Terminating impedance	UNBALANCED–BALANCED 50/50			ohm
VSWR			2.0	
Maximum drive level			+15	dBm

Part no: NMP code 4511049

1st mixer in CRFU_1a

Parameter	Min.	Typ./ Nom.	Max.	Unit/Notes
Supply voltage	2.7	2.8	2.85	V
Current consumption		9		mA
RX frequency range	935		960	MHz
LO frequency range	1006		1031	MHz
IF frequency		71		MHz
Insertion gain	9		12	dB
NF, SSB			11.5	dB
IIP3	0			dBm
1 dB input compression point	–10			dBm
IF/2 spurious level	–30			dBm, *
LO power level in RF–port			–25	dBm
Input VSWR			2	
Output resistance (balanced)	10 k			ohm
Output capacitance (balanced)		1.2		pF

1st IF–filter

Parameter	min.	typ.	max.	unit
Operating temperature range	–20		+75	deg.C
Center frequency , fo		71		MHz
Maximum ins. loss at 1dBBW			11	dB
Group delay ripple at +/–90 kHz BW			1.3	us pp
Bandwidths relative to 71 MHz 1 dB bandwidth 3 dB bandwidth 5 dB bandwidth 22 dB bandwidth 30 dB bandwidth 40 dB bandwidth	 +/– 70 +/–120		 +/– 230 +/– 350 +/– 550 +/– 700	kHz
Spurious rejection, fo +/– 26 MHz	65			dB, *
Terminating impedance (balanced) resistance input resistance output capacitance (parallel) input capacitance (parallel) output		 1.1 1.2 15.6 10.6		 kohm kohm pF pF

* Matching network included. NMP part no. 4510137

AGC–stage and 2nd mixer in SUMMA

Parameter	Min.	Typ.	Max.	Unit/Notes
Supply voltage	2.7	2.8	2.85	V
Current consumption		27	32	mA
Input frequency range	45		120	MHz
2nd IF frequency range	0.4		17	MHz
Total noise figure, SSB, max. gain			15	dB,
Total noise figure, SSB, min. gain			65	dB,
Max. voltage gain	40			dB
Min. voltage gain			–20	dB
Control voltage for min. gain		0.5		V
Control voltage for max. gain		1.4		V
Output 1 dB compression point @ max. gain	800			mVpp
Input 1 dB compresion point @ min. gain	80			mVpp
IF input impedance (balanced)	2.4/tbd	3.8/2	5.6/tbd	kohm/pF
2nd mixer output impedance (single output)			100	ohm

2nd IF Filter

Parameter	min.	typ.	max.	unit
Center frequency, fo		13		MHz
1 dB bandwidth, 1dBBW (relative to 13 MHz)	+/– 90			kHz
Insertion loss			6.0	dB
Amplitude ripple at 1dBBW			1.0	dB
Group delay ripple at 1 dB BW, peak to peak			1.5	us
Attenuations, relative to 13 MHz fo +/– 400 kHz fo +/– 600 kHz fo +/– 800 kHz	 25 35 45			dB
Terminating impedance	313	330	347	ohm

NMP part no. 4510009

Buffer in SUMMA for 2nd IF

Parameter	Min.	Typ.	Max.	Unit
Input frequency range	0.4		17	MHz
Voltage gain (single ended input and balanced output)	34	36	38	dB
1 dB output compression point (Rload=10 kohm balanced)		1.4		Vpp
Input impedance		3.3/4		kohm/pF
Output impedance, balanced			600	ohm

Transmitter blocks

IQ–modulator and TX–AGC in SUMMA

Parameter	Min.	Typ.	Max.	Unit
Supply voltage	2.7	2.8	2.85	V
Current consumption		28	tbd.	mA
Modulator Inputs (I/Q)	**Minimum**	**Typical / Nominal**	**Maximum**	**Unit / Notes**
Input bias current (balanced)			100	nA
Input common mode voltage		0.8		V
Input level (balanced)			1.2	Vpp
Input frequency range	0		300	kHz
Input resistance (balanced)	tbd			kohms
Input capacitance (balanced)			2	pF
IQ–input phase balance total, temperature included	–4		4	deg.
IQ–input phase balance temperature effect	–2		2	deg.
IQ–input amplitude balance total, temperature included	–0.5		0.5	dB
IQ–input amplitude balance temperature effect	–0.2		0.2	dB
Modulator Output	**Minimum**	**Typical / Nominal**	**Maximum**	**Unit / Notes**
Output frequency	85		400	MHz
Output power, high (balanced, into 100 ohm) NOTE: Requires input level of 1.1 Vpp (difrential)	–5	–3		dBm
Output power, low (balanced, into 100 ohm) NOTE: Requires input level of 1.1 Vpp (diff.)	–10	–8		dBm
Noise level in output			–145	dBm/Hz avg.
Total gain control range	35			dB
Gain step		5		dB

Modulator Output	Minimum	Typical / Nominal	Maximum	Unit / Notes
Absolute gain accuracy	–2		+2	dB
Any gain step up/down settling time			10	usec
Output 3rd Order Intermodulation products, when both wanted signals are at the level of –12 dBm at the output			–35	dB

116 MHz LC TX IF–filter

Parameter	Min.	Typ.	Max.	Unit
Center frequency		116		MHz
Insertion loss @ 116 MHz			3.7	dB
Relative attenuation @ +/– 10 MHz offset	5			dB
Relative attenuation @ +/– 20 MHz offset	8			dB
Relative attenuation @ 232 MHz	15			dB
Relative attenuation @ 348 MHz	20			dB
Relative attenuation @ 464–1000 MHz	25			dB
Input impedance, balanced		100		ohm
Output impedance, balanced		200		ohm

Upconversion mixer and in CRFU_1a

Parameter	Min.	Typ.	Max.	Unit
Supply voltage	2.7	2.8	2.85	V
Supply current			50	mA
Input frequency		116		MHz
Input level		–5	–8	dBm
Output frequency range	890		915	MHz
Output level	+3	+5		dBm
NF,SSB			20	dB
LO–signal level in output			–29	dBc
Unwanted sideband level			–15	dBc
fLO+/–2xIF spurious level			–40	dBc
7x116 MHz spurious level			–40	dBc

Parameter	Min.	Typ.	Max.	Unit
8x116 MHz spurious level			–55	dBc
Input impedance (balanced)		600//2		ohm//pF
Output VSWR, (with matching network and output balun)			2	

TX interstage filter

Parameter	Min.	Typ.	Max.	Unit
Passband	890 – 915			MHz
Insertion loss			3.8	dB
Ripple in passband			1.5	dB
Attenuation DC...813 MHz	35			dB
Attenuation 925...935 MHz	7			dB
Attenuation 935...960 MHz	15			dB
Attenuation 1006...1031 MHz	40			dB
Attenuation 1122...1147 MHz	45			dB
Attenuation 1780...1830 MHz	10			dB
Attenuation 2670...2745 MHz	10			dB
Terminating impedance		50		ohm
VSWR			2.5	
Maximum drive level			+15	dBm

NMP part no. 4511015

Power amplifier MMIC

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Operating freq. range			880		915	MHz
Supply voltage	Vcc		3.0	3.5	5.0	V
Auxiliary supply voltage	Vreg		2.7	2.8	2.9	V
Auxiliary supply current	Ireg				tdb.	mA
Input power	Pin	Pout=35.0 dBm, Vcc=3.5 V, Vpc=2.2 V,	0	2	5	dBm
Output power	Pout	Pin= 0 dBm, Vcc=3.0 V, Vpc=2.2 V, Tamb=+85 deg.C	34.2			dBm
Gain control range (overall dynamic range)		Vpc= 0.5 ... 2.2 V	45			dB
Gain control slope (sensitivity at the linear range)	S	Vpc1 @10 Vpeak output volt. Vpc2 @0.5 Vpeak output volt. S=((10–0.5)/(Vpc1–Vpc2)) V/V, Pin = 0...+5dBm	20	tbd.	40	V/V

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Isolation		Vcc=3.5 V, Vpc=0.2 V, Pin=0 dBm			–40	dB
Carrier switching time	tr, tf	Vcc=3.5 V, Pin=0 dBm Vpc is a pulse from 0.2 to 2.2 V. Rise time up to –0.5 dB from the final power. Fall time vice versa.			1	us
Total efficiency	η	Pin= 0 dBm , Pout= +34.3 dBm, Vcc=3.5 V, Tamb = + 25 deg. C	50			%
Control current	Ipc	Pin= 0...+5 dBm , Pout= +34.8 dBm, Vcc=3.5 V			+/– 3	mA peak
Harmonics					–35	dBc
Input VSWR	VSWRi1	Pin= 0...+5 dBm , Pout= +34.0 dBm, Vcc=3.5 V			2:1	
	VSWRi2	Pin= 0...+5 dBm , Pout= +6.0 ... +32.0 dBm, Vcc=3.5 V Vpc adjusted for desired power levels			4:1	
Leakage current	Ileak	Vcc=3.5 V, Vpc=0 V, Vreg=0 V, no RF–drive			10	uA
Intermodulation distortion	IMD	Pinwant= 0 dBm @ 915 MHz Pinint = –50 dBm @ 905 MHz Poutwant= +34.8 dBm Vcc=3.5 V, Poutint @905 MHz Poutimd @925 MHz IMD=Poutint – Poutimd, Tamb = + 25 deg. C	5			dB
AM–PM conversion	Kp	Pin= –2.0 ... +5.0 dBm, Pout= +6.0 ... +34.0 dBm Vpc adjusted for desired output power levels Vcc=3.0 V			3	deg/dB
Receive band noise power	Pn	Vcc=3.5 V , RBW=30kHz Pout = +34.8 dBm, Freq. band: 925...960 MHz			–80	dBm
Stability		Pin= 0 dBm+/–3dBm, Vcc=3.0...5.0 V, Vpc=0 ... 2.2 V Load VSWR 12:1, all phases	All spurious outputs more than 65 dB below desired signal			
Load mismatch stress		Pin= 0 dBm, Vcc=5.0 V, Pout=Pmax Load VSWR 20:1, all phases	No module damage			

Directional coupler

Parameter	Min.	Typ.	Max.	Unit/Notes
Frequency range	890		915	MHz
Insertion loss			0.5	dB
Coupling factor		15		dB
Directivity	13		14	dB
Impedance level of the main line		50		ohm
VSWR on main line			1.6	
Impedance level of the coupled line		50		ohm

NMP part no. 4551001

Power detector

Parameter	Min.	Typ.	Max.	Unit/Notes
Supply voltage	2.7	2.8	2.85	V
Supply current			2.0	mA
Frequency range	890		915	MHz
Dynamic range	45			dB
Linear range, *	35			dB
Bias current for detector diode		40		uA
Input power range, **	–8		20	dBm
Output voltage	0.1		2.2	V
Variation of the detected voltage over temperature range			0.7	mV/°C
Load resistance	10			kohm

* RF input voltage versus detected output voltage
* * Directional coupler coupling factor 14 dB

Power control section in SUMMA, closed loop characteristics

Parameter	Min.	Typ.	Max.	Unit/Notes
Supply voltage	2.7	2.8	2.85	V
Supply current		tbd.		mA
TXP input voltage, LOW			0.5	V
TXP input voltage, HIGH	2.4			V
Detector input voltage	0.1		2.2	V
TXC input voltage	0.1		2.2	V

Parameter	Min.	Typ.	Max.	Unit/Notes
TXC and TXP input resistance	50			kohm
TXC and TXP input capacitance		4		pF
Output voltage (POP & POG)	0.5		2.2	V
POP– and POG–output impedance		50		ohm
POP and POG –output current driving capability	+/– 4			mA
Switch on resistance (bet–ween INL& POP or POG)		tbd.		ohm
Voltage of POP/POG when inactive (max. 3.5mA sink)		0.1		V
Offset of OP1 and OP2 op.amp.	–40		40	mV
Temperature coefficient of the offset voltage		30		uV/deg.C
Bandwidth (OP1 & OP2), unity gain	6			MHz
Open loop gain		20		dB
Closed loop gain		15		dB
Closed loop –3 dB bandwidth		70		kHz
Phase margin	45	60		degrees
Gain margin		30		dB

Synthesizers blocks

VCTCXO, reference oscillator

Parameter	Min.	Typ.	Max	Unit/.Notes
Supply voltage, Vcc	2.70	2.80	2.85	V
Current consumption, Icc			1.5	mA
Operating temperature range	–20		+75	deg. C
Nominal frequency		13		MHz
Output voltage swing (swing of 13 MHz component, selective measurement from the spectrum)	800			mVpp
Load, resistance capacitance		2 10		kohm pF
Frequency tolerance @+25 deg. C	– 1.0		+ 1.0	ppm
Frequency tolerance after reflow (@ +25 deg. C)	– 2.0		+ 2.0	ppm

Parameter	Min.	Typ.	Max	Unit/.Notes
Frequency stability vs. temperature (ref. @+25 , –20....+75 deg. C)	– 5.0		+ 5.0	ppm
Frequency stablity vs. supply voltage (2.8 V +/– 100 mV)	– 0.1		+ 0.1	ppm
Frequency stability vs. load change (2 kohm//10 pF +/– 10 %)	– 0.3		+ 0.3	ppm
Aging	– 1.0		+ 1.0	ppm/year
Nominal control voltage, Vc		1.15		V
Voltage control range	0.0		2.3	V
Voltage control characteristics (see note 1.)	+/– 12		+/– 24	ppm/V when 0.3 V<Vc<2.3 V
Vc input resistance	1			Mohm
Frequency adjustment	+/– 3.0			ppm with inter– nal trimmer
Harmonics (with 2 kohm//10 pF)			– 5	dBc
Start up time output level within 90% output frequency limits +/–0.05ppm from the final value			 5 5	ms
Phase noise @ 1 kHz offset			–130	dBc/Hz

VHF PLL in SUMMA

The same VHF VCO and also the same frequency is used so the VHF PLL is common.

Table 2. VHF–synthesizer, specification

Parameter	Min.	Typ.	Max.	Unit/Notes
Start up settling time			3.0	ms
Phase error			1	deg./rms
Sidebands +/– 1 MHz +/– 2 MHz +/– 3 MHz > +/– 3.0 MHz			 –70 –80 –80 –90	 dBc

Table 3. VHF PLL block in SUMMA, specification

Parameter	Min.	Typ.	Max.	Unit/notes
Input frequency range	150		500	MHz
Input signal level	80		800	mVpp
Input resistance	tbd.			kohm
Input capacitance			tbd.	pF
Supply current		3.5		mA
Reference input frequency			30	MHz

Table 3. VHF PLL block in SUMMA, specification (continued)

Parameter	Min.	Typ.	Max.	Unit/notes
Phase comparison frequency			1	MHz
Charge pump output current 1 current 2		 0.5 2.0		mA
Sink to source current matching error of the charge pump			+/– 5	%
Charge pump current error			+/– 10	%
Charge pump min. output voltage		0.5		V
Charge pump max. output voltage		* Vcp–0.5		V
Charge pump leakage current			5	nA
Phase detector phase noise level			–163	dBc/Hz

*Vcp = 5V

VHF VCO and low pass filter

Parameter	Min.	Typ.	Max.	Unit/Notes
Supply voltage range	2.7	2.8	2.85	V
Current consumption		4	7	mA
Control voltage	0.5		4.0	V
Operation frequency		232		MHz
Output level	–13	–10		dBm (output after the lowpass filter)
Harmonics			–30	dBc, (filtered)
Phase noise, fo +/– 600 kHz fo +/– 1600 kHz fo +/– 3000 kHz			 –120 –130 –140	dBc
Control voltage sensitivity	8.0		14.0	MHz/V
Pushing figure			+/– 2	MHz/V
Frequency stability			+/– 3	MHz (over temperature range –10...+75 C deg.)
Spurious content			–70	dBc

UHF PLL

Table 4. UHF–synthesizer,

Parameter	Min.	Typ.	Max.	Unit/Notes
Start up settling time			3.0	ms
Settling time +/– 25 MHz		500	800	us, (into +/– 20 Hz from final frequency)
Phase error			3.7	deg./rms
Sidebands +/– 200 kHz +/– 400 kHz +/– 600...+/–1400 kHz +/–1.4... +/– 3.0 MHz > +/– 3.0 MHz			 –40 –60 –66 –76 –86	 dBc

Table 5. UHF PLL block in SUMMA

Parameter	Min.	Typ.	Max.	Unit/notes
Input frequency range	650		1700	MHz
Input signal level (f<1.5 GHz)	200			mVpp
Input resistance	tbd.			kohm
Input capacitance			tbd.	pF
Supply current		8		mA
Reference input frequency			30	MHz
Reference input level	100			mVpp
Reference input impedance		tbd.		
Phase comparison frequency			1	MHz
Charge pump output current 1 current 2		 0.5 2.0		 mA
Sink to source current matching error of the charge pump			+/– 5	%
Charge pump current error			+/– 10	%
Charge pump current temperature variation			tbd.	%
Charge pump leakage current			5	nA
Phase detector phase noise level			–163	dBc/Hz

UHF VCO module

Parameter	Conditions	Rating	Unit/ Notes
Supply voltage, Vcc		2.8 +/– 0.1	V
Supply current, Icc	Vcc = 2.8 V, Vc= 2.25 V	< 10	mA
Control voltage, Vc	Vcc = 2.8 V	0.8... 3.7	V

Parameter	Conditions	Rating	Unit/ Notes
Oscillation frequency	Vcc = 2.8 V Vc = 0.8 V Vc = 3.7 V	 < 1006 > 1031	 MHz MHz
Tuning voltage in center frequency	f = 1018.5 MHz	2.25 +/– 0.25	V
Tuning voltage sensitivity in operating frequency range on each spot freq.	Vcc = 2.8 V f=1006...1031 MHz	14 +/– 2	MHz/V
Output power level	Vcc=2.7 V f=1006...1031 MHz	–6.0 min.	dBm
Output impedance and VSWR	f=1006...1031 MHz	50 ohms,VSWR <2	
Phase noise, fo +/– 25 kHz fo +/– 600 kHz fo +/– 1600 kHz fo +/– 3000 kHz	Vcc=2.8 V f=1006...1031 MHz	–100 –120 –130 –140	dBc/Hz max.
Pulling figure	VSWR=2, any phase	+/– 1.0	MHz max.
Pushing figure	Vcc=2.8 +/– 0.1 V	+/– 2.0	MHz/V max.
Frequency stability over temperature range	Ta=–20 ... +75 deg. C	+/– 3.0	MHz max.
Harmonics		–10 max.	dBc
Spurious	Vcc=2.8 V, Vc=0...6 V	–70 max.	dBc
Input capacitance in Vc–pin	Vc= 0 V	100 max.	pF

UHF local signal input in CRFU_1a

Parameter	Min.	Typ.	Max.	Unit/Notes
Input frequency range	990		1040	MHz
Input level	200		700	mVpp
Input resistance		100		ohm
Input capacitance			1.5	pF

RF/BB/DSP Interface

The following three sections describe the hardware and timing interface between RF and the BB/DSP section of the RAE–2.

Interface Signal Characteristics

The interface signals between the BB and the RF section are shown in the next table as a logical interface. On physical board level baseband supplies voltages from CCONT to separate RF sub–blocks. The maximum values specified for the digital signals in the table are the absolute maximum values from the RF interface point of view.

Table 6. AC and DC Characteristics of RF/BB signals

Signal name	From - To	Function
VBATT	Battery RF	Supply voltage for RF (PA on/PA off)
VXOENA	MAD CCONT	VR1, VR6 in CCONT ON
		VR1, VR6 in CCONT OFF
SYNPWR	MAD CCONT	VR3, VR4 in CCONT ON
		VR3,VR4 in CCONT OFF
RXPWR	MAD CCONT	VR2, VR5 in CCONT ON
		VR2, VR5 in CCONT OFF
TXPWR	MAD CCONT	VR7 in CCONT ON
		VR7 in CCONT OFF
VREF	CCONT SUMMA	Reference voltage for SUMMA and CRFU1a
PDATA0	MAD CRFU1A	Nominal gain in LNA
		Reduced gain in LNA
SENA	MAD SUMMA	PLL enable
SDATA	MAD SUMMA	Synthesizer data
SCLK	MAD SUMMA	Synthesizer clock
AFC	COBBA VCTCXO	Automatic frequency control signal for VC(TC)XO
		10...10000Hz
RFC	VCTCXO MAD	High stability clock signal for the logic circuits
RXIP/RXIN	SUMMA COBBA	Differential RX 13 MHz signal to baseband
TXIP/TXIN	COBBA SUMMA	Differential in–phase TX baseband signal for the RF modulator
TXQP/TXQN	COBBA SUMMA	Differential quadrature phase TX baseband signal for the RF modulator
TXP	MAD SUMMA	Transmitter power control enable

Table 6. AC and DC Characteristics of RF/BB signals (continued)

Signal name	From - To	Function
TXC	COBBA SUMMA	Transmitter power control
		0...200 kHz
RXC	COBBA SUMMA	Receiver gain control
		0...200 kHz

TXC and AGC signals originate from the same DAC, controlled in COBBA

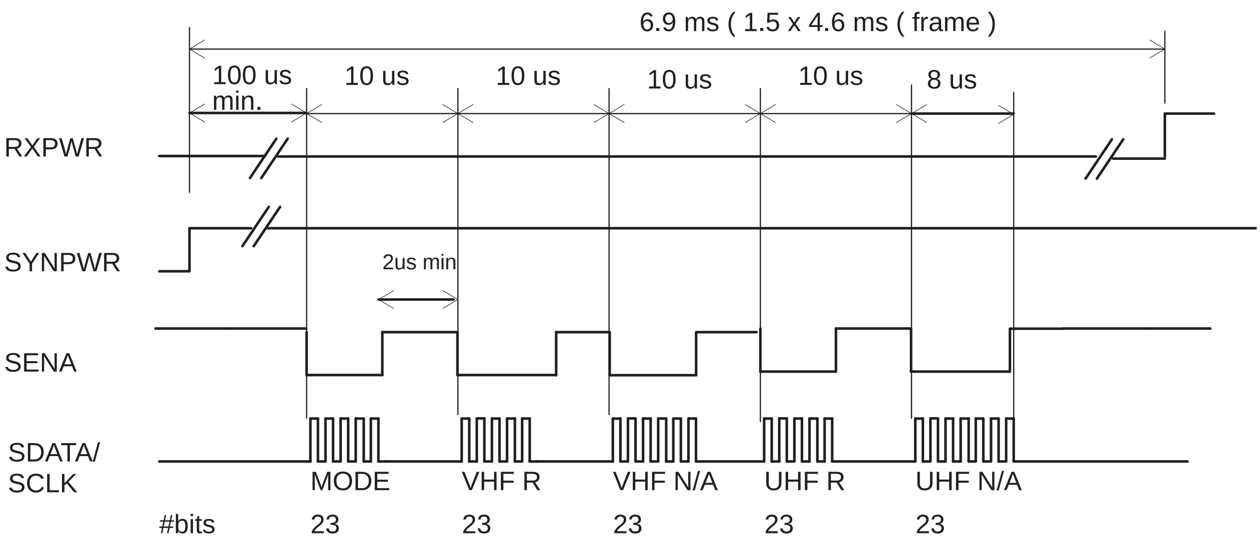
Data Interface and Timing

The SUMMA is programmed via the serial bus SENA, SDATA and SCLK. The data of the SDATA is clocked by rising edge of SCLK. The data is fed MSB first and address bits before data bits. The data for the Programmable dual modulus counter is fed first and the Swallow counter last. SENA is kept low while clocking the data. (Figure below)

During programming, the charge pump attached to programmed divider is switched to high impedance state. Also all counters connected to the PLL that is programmed, are kept on reset while the SENA is low.

Table 7. Logic levels

Parameters	Min	Typ	Max	Units
High	2			Volt
Low			0.8	Volt



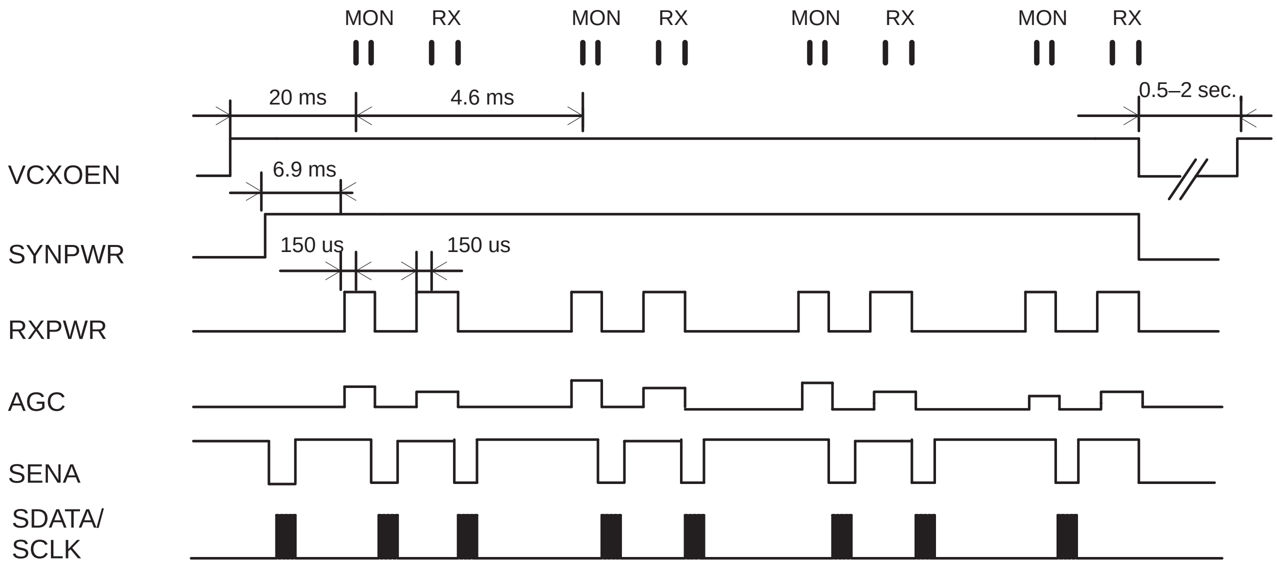


Figure 3. Synthesizer timing / IDLE, one monitoring/frame, frame can start also from RX–burst

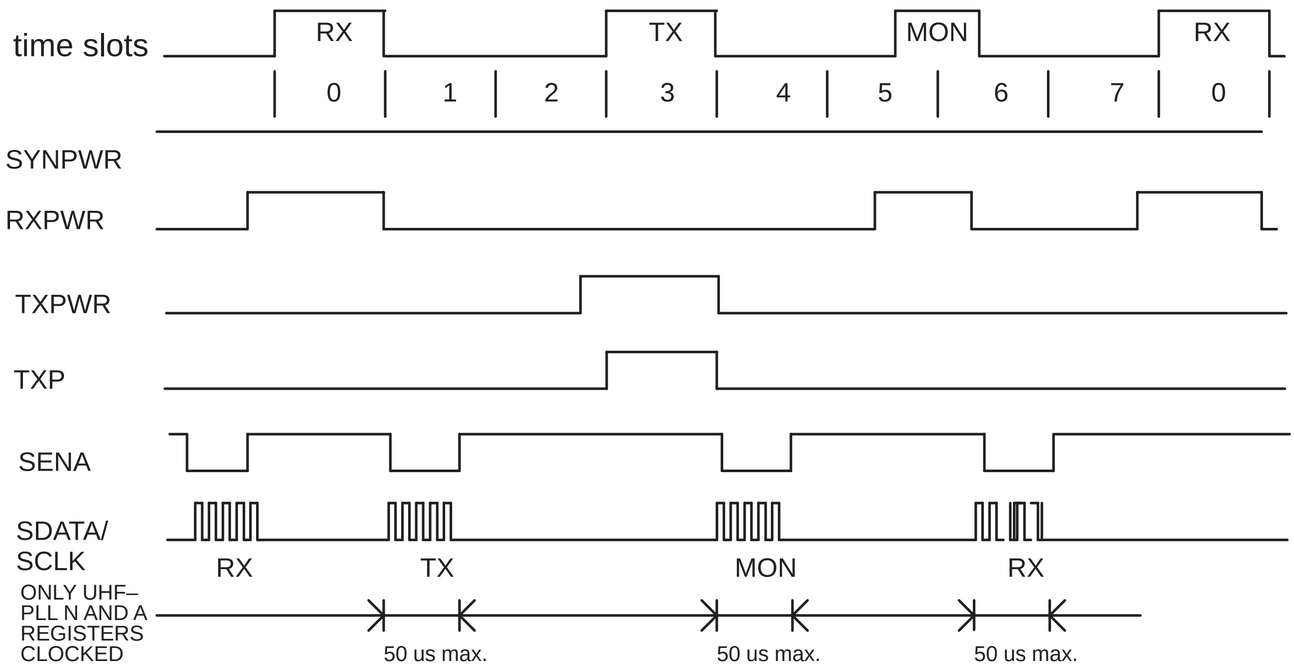


Figure 4. UHF–synthesizer timing/clocking on traffic channel

Transmit Power Timing

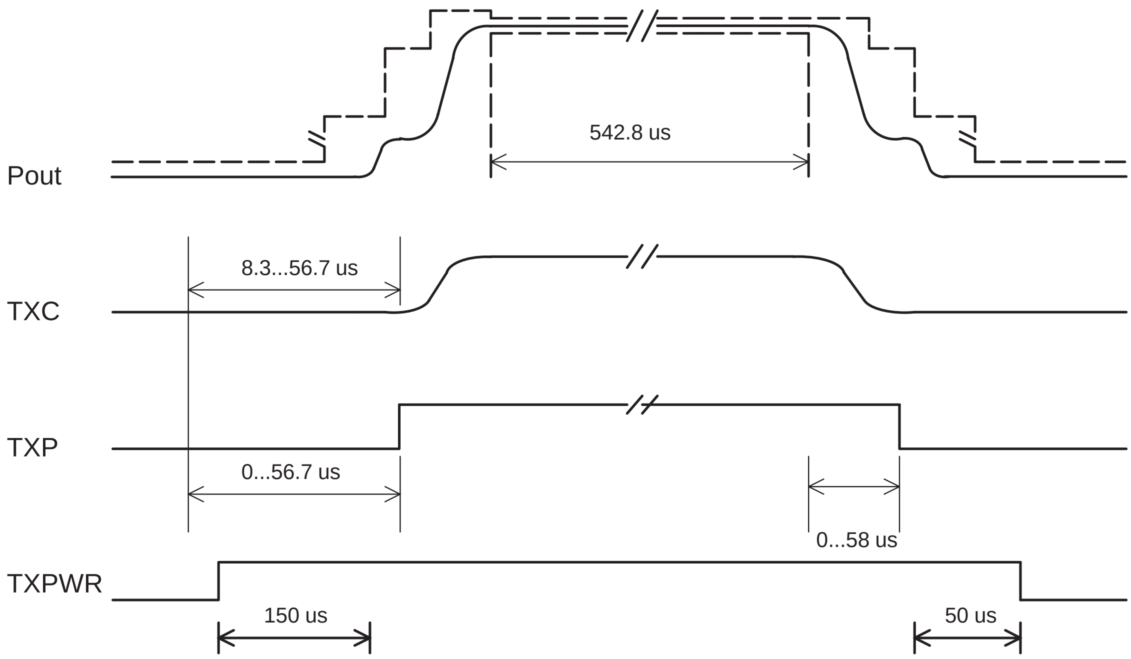


Figure 5. Transmitter timing diagram for normal bursts

SUMMA and Synthesizer Control

Registers

The following table shows the programmable registers in SUMMA which are used for programmable counters and mode selection.

Table 8. Registers addressing

A2	A1	A0	HEX addr.	Bits	Register
0	0	0	0	18	Control register
0	0	1	1	15	VHF VDIV (VDIV2)
0	1	0	2	12	VHF RDIV (RDIV2)
0	1	1	3	18	UHF VDIV
1	0	0	4	12	UHF RDIV

PLL Control Word Format

Serial data format is shown below. Amount of bits needed for each address can be seen from Table 2. **When less bits are sent, dummy bits must be inserted between the address and the real data**.

MSB													LSB
A2	A1	A0	...	...	S9	S8	S7	S6	S5	S4	S3	S2	S1

Control Register

Bit no	Sign.	BS8 Def.	Name	Purpose
S1	LSB	0	VHFOFF	1=VHF synth power down
S2		0	NF	No Function
S3		1	MODE1	Mode selection LSB
S4		0	MODE2	Mode selection MSB
S5		0	TEST	Test Mode selection
S6		0	VHFCPCS	VHF charge pump current Set = 0 (0.5 mA) 1(2.0 mA)
S7		0	UHFCPCS	UHF charge pump current Set 0 (0.5 mA) 1(2.0mA)
S8		0	VPDMOD	Logic high keeps counters reset
S9		0	ADDBIAS	Extra bias for UHF prescaler
S10		1	G1	TX AGC step
S11		0	NF	No Function

Bit no	Sign.	BS8 Def.	Name	Purpose
S12		0	NF	No Function
S13		0	NF	No Function
S14		1	fast	Add current to chargepump
S15		0	PD_lin	UHF Phase detector mode
S16		0	UHFOFF	1=UHF synthesizer power down
S17		0	RX_SEL	digital RX on
S18		1	OA_sel	Selects pwrctrl opamp
S19	MSB	1	TX_AGC_LATCH	TXP driven agc gain latching

NOTE: NDIV2 divides reference frequency by programmable figure of 2–2047. Divide ratio less than 2 is prohibited.

Synthesizer clocking

GSM Division ratios

The values of ch range from 1 to 124

UHF synthesizer

reference divider ratio	R=65
N counter division ratio	N=INT((ch + 5030)/64)
A counter division ratio	A=MOD((ch + 5030)/64)

VHF synthesizer

reference divider ratio	R=13
N counter division ratio	N=14
A counter division ratio	A=8

Clocking scheme

During power up (first clocking) SUMMA synthesizers should be enabled in the following order :

1. Mode setting (GSM)
2. reference divider for VHF PLL
3. N and A dividers for VHF PLL
4. reference divider for UHF PLL
5. N and A dividers for UHF PLL

When transceiver is on allocated channel, then only (N and A dividers) UHF PLL is controlled, because it is the channel synthesizer. Mode settings and VHF PLL division ratios are fixed.

List of abbreviations

ADC	Analog to Digital Converter
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
AM	Amplitude Modulation
ASIC	Application Specific Integrated Circuit
AVG	Average
BB	Baseband
BiCMOS	Bipolar and Complementary Metal Oxide Semiconductor process
BT	Bandwidth x symbol time (GMSK filter parameter)
BW	Bandwidth
CCONT	DCT3 power management ASIC
CLK	Clock
COBBA	DCT3 RF/BB and audio interface ASIC
CRFU1A	DCT3 dualband RF ASIC
CW	Continuous Wave
DAC	Digital to Analog Converter
DC	Direct Current
DCS	Digital Cellular System
DCT	Digital Core Technology
DSP	Digital Signal Processing or Digital Signal Processor
E–GSM	Extended GSM (wider TX/RX bands)
ESD	Electrostatic Discharge
ESR	Effective Series Resistance
ETSI	European Telecommunications Standard Institute
FDMA	Frequency Division Multiple Access
FIR	Finite Impulse Response
GMSK	Gaussian Minimum Shift Keying
GND	Ground
GSM	Global System for Mobile communications
HT	Hilly Terrain (GSM standard fading profile)
IC	Integrated Circuit
IF	Intermediate Frequency
IIP3	3rd order intermodulation Input Intercept Point

IMD	Intermodulation Distortion
LNA	Low Noise Amplifier
LO	Local Oscillator
MAD	DCT3 DSP/MCU/system logic ASIC (**M**CU–**A**SIC–**D**SP)
MMIC	Monolithic Microwave Integrated Circuit
MON	Monitoring slot
MS	Mobile Station
NF	Noise Figure
OIP3	3rd order Output Intercept Point
PA	Power Amplifier
PCB	Printed Circuit Board
PLL	Phase Locked Loop
PM	Phase Modulation
RA	Rural Area (GSM standard fading profile)
RBW	Resolution Bandwidth
RF	Radio Frequency
RMS	Root Mean Square
RSSI	Received Signal Strength Indicator
RX	Receiver
RXLEV	RX Level
SAW	Surface Acoustic Wave
SACCH	Slow Associated Control Channel
SPR	Standard Product Requirements (NMP’s internal standard)
SSB	Single Sideband
SUMMA	DCT3 dualband IF ASIC
TCH	Traffic Channel
TDMA	Time Division Multiple Access
TU	Typical Urban (GSM standard fading profile)
TX	Transmitter
UHF	Ultra High Frequency (300 MHz ... 3 GHz)
VCO	Voltage Controlled Oscillator
VCTCXO	Voltage Controlled Temperature Compensated Crystal Oscillator
VHF	Very High Frequency (30 MHz ... 300 MHz)
VSWR	Voltage Standing Wave Ratio

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